PRISM1RC-EVAL - 2.4GHz MACless DSSS Radio User's Guide

Application Note | **November 1998** | **AN9808.2**

Authors: Bob Rood, Milutin Culibrk

Introduction

The Radio Card product provides all the hardware required to implement wireless communication using Direct Sequence Spread Spectrum (DSSS) technology. Only an external Media Access Controller is required.

DSSS technology provides interference rejection in the presence of narrow band noise. Since the output power is spread across such a large bandwidth, the DSSS signal is low level and wide bandwidth and therefore not intrusive to other equipment.

Evaluation kits include two MACless cards in a PCMCIA Type II form factor and users guide AN9808. The PRISM1RC-EVAL MACless radio kit does not include any software.

THE PCMCIA BUS INTERFACE HAS NOT BEEN IMPLEMENTED IN THIS CARD, THEREFORE A PROPER INTERFACE IS REQUIRED, (SEE SIGNAL DESCRIPTION).

This product has been designed to allow evaluation of the Intersil PRISM Direct Sequence chip set.

The PRISM1RC-EVAL is not FCC approved as an intentional radiator and is intended for use with cabled connections only (30dB attenuation recommended antenna port to antenna port). An FCC experimental license is required while transmitting over the air with unapproved equipment.

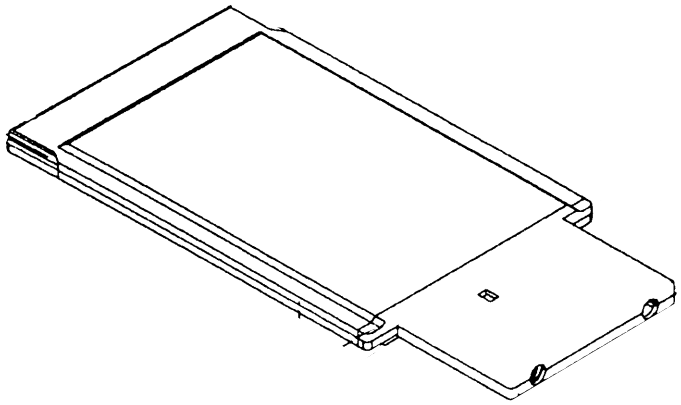
Features

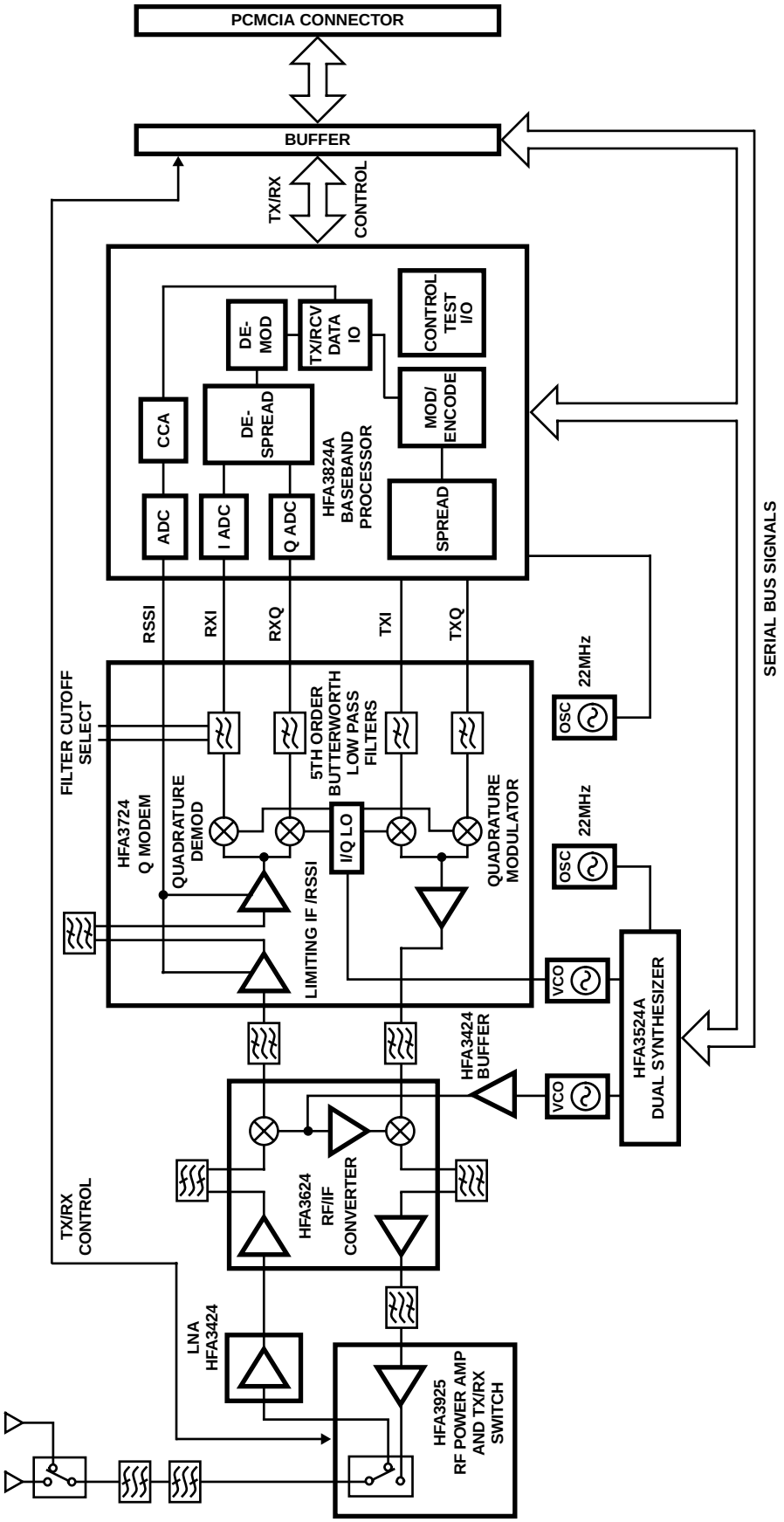
- Provides Antenna-to-Bits Data Stream
- Single Heterodyne Conversion
- Programmable Antialiasing and Shaping Filters
- Autonomous Half Duplex Direct Sequence Modem
- Selectable DBPSK, DQPSK Signalling
- Antenna Diversity Selection
- Differential Data Encoding/Decoding
- Programmable 16-Bit PN Code
- Data Rates Up to 2Mbps DQPSK Standard
- Data Rates Up to 4Mbps DQPSK with Modifications
- Power Management Control
- Low Profile PCMCIA PC Card Type II

Ordering Information

PART NUMBER	DESCRIPTION	CARDS PER KIT
PRISM1RC-EVAL	Evaluation Kit	2

Packaging



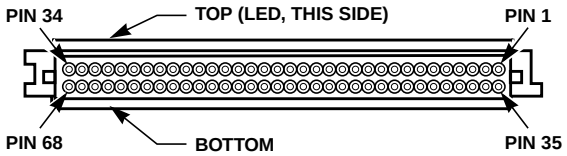


PRISM1RC-EVAL Block Diagram

Connector Pin Assignment

SIGNAL NAME	PCMCIA PIN NUMBER
GND	1, 34, 35 and 68
Unused	2-10, 15, 16, 31, 32, 37-58, 60, 61, 64-66, 18 and 52
OSC_START	11
RX_PE_BB	12
BB_AS	13
BB_CS	14
V_{CC}	17 and 51
BB_RD/WR	19
CLK/SYNTH_CLK	20
SYNTH_LE	21
SEL0	22
SEL1	23
RADIO_PE	24
PA_PE	25
RESET_BB	26
RX_PE	27
TXDATA	28

SIGNAL NAME	PCMCIA PIN NUMBER
TX_PE	29
SD/SYNTH_DATA	30
TXC	33
RXCIN	36
SPCSPWR (Future)	40
RADCLK (Future)	41
TX_PE3 (Future)	42
SYNTH_LD (Future)	43
MD_RDY	59
CCA	62
RXDATA	63
TX_RDY	67



CONNECTOR VIEW

Operating Conditions

Voltage . . . . . .4.5V to 5.5V
Temperature Range . . . . . .0^{o}C to 55^{o}C

DC Electrical Characteristics

Current Consumption

Average Current
- Without Power Saving Mode [3] . . . . . 225mA (Typ)
  2% Transmit, 98% Receive
- With Power Saving Mode [3]. . . . . 53mA (Typ)
  2% Transmit, 8% Receive, 90% Standby

Continuous Receive Mode [3] . . . . . 221mA (Typ)
Continuous Transmit Mode [3] . . . . . 422mA (Typ)
Standby Mode [3] . . . . . 30mA (Typ)

Input/Output Characteristics

Input LOW Level. . . . . .0.8V (Max)
Input HIGH Level . . . . . 2.0V (Min)
Output LOW Level
- V_{OL} (I_{OL} = 0.1mA) . . . . . .0.2V (Max)
- V_{OL} (I_{OL} = 24mA). . . . . .0.5V (Max)

Output HIGH Level
- V_{OH} (I_{OH} = -3mA). . . . . .2.4V (Min) to 3.0V (Typ)
- V_{OH} (I_{OH} = -0.1mA) . . . . . V_{CC}-0.2V (Min)

Input LOW Current (V_{CC} = Max) . . . . . .±5µA (Max)
Input HIGH Current (V_{CC} = Max). . . . . .±5µA (Max)
Output Capacitance . . . . . .8.0pF (Max)
Input Capacitance . . . . . .8.0pF (Max)

RF System Characteristics

Output Power (25^{o}C) . . . . . 15dBm (Min)
Transmit Spectral Mask . . . . . -32dBc (Typ) at First Sidelobe
Receive Sensitivity . . . -89dBm (Typ) 1 Mbps DBPSK 8% PER
. . . . . -86dBm (Typ) 2 Mbps DQPSK 8% PER
Input Third Order Intercept . . . . . -22dBm (Typ)
Image Rejection . . . . . .65dB (Typ) 8% PER
IF Rejection . . . . . .80dB (Typ) 8% PER
Adjacent Channel Rejection . . . . . .63dB (Typ) 8% PER
at 25MHz Offset

Functional Overview

The Radio Card is based on the Intersil PRISM Direct Sequence Chip Set.

There are ten basic units in this card:

1. Baseband Processor
2. Modulator/Demodulator
3. Dual Synthesizer
4. Up/Down Converter
5. Power Amplifier
6. Low Noise Amplifier (LNA)
7. RF VCO
8. IF VCO
9. Antenna
10. Buffer Interface

During transmission, the data to be transmitted should be placed on the TX data line going into the baseband processor. This data will be modulated according to the format selected (DBPSK or DQPSK) and then spread using a programmable PN code. Two signals will be generated (I & Q).

The I & Q signals are sent to the Modulator/Demodulator where they will be first filtered and then modulated with the IF frequency (280MHz). The IF oscillator generates 560MHz which is divided by two inside the Modulator/Demodulator, so the final IF signal is 280MHz. Next, the two signals are combined into a single signal and sent over to the Up/Down converter.

The Up/Down converter will shift this signal to the RF channel programmed in the synthesizer, in the 2.4GHz ISM band.

In the final stage this signal is amplified to produce a power output of 15dBm minimum measured at the antenna.

In the receive mode, the radio signal is received by the antenna, amplified by the LNA, and placed into the Up/Down converter. The Up/Down converter will down-convert this signal from the 2.4GHz range to the IF frequency (280MHz).

The Modulator/Demodulator then splits the signal into the I & Q form, before it is sent to the baseband processor.

Finally, the baseband processor despreads and demodulates the data from DBPSK or DQPSK form, and places it on the RX data line.

The buffer translator is used to interface between 5V and 3.5V logic.

The RF and IF Local Oscillator signals are generated using the synthesizer and the voltage controlled oscillators. The dual synthesizer should be programmed with the desired RF channel frequency less the IF frequency.

Example:

	RF		IF		LO
CH1	2412MHz	-	280MHz	=	2132MHz

The baseband processor and the synthesizer are driven by two 22MHz oscillators to control the timing of these chips.

Refer to Application Note AN9624 [1] for a more detailed radio description.

Edge Connector Pin Descriptions

The block diagram in Figure 1 shows control signal connections from the edge connector to the radio integrated circuits.

PA_PE (I) Pin 25

When active high the baseband processor and power amplifier are in transmit mode, otherwise they are in standby mode (see Figure 6).

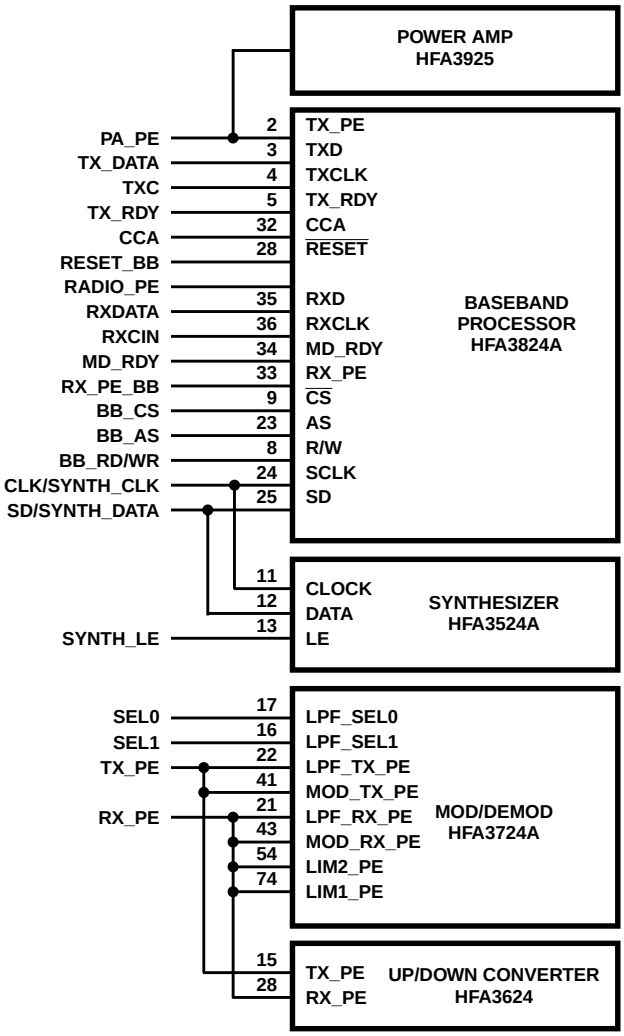


FIGURE 1. CONTROL SIGNAL CONNECTIONS

This signal is usually obtained from a MAC or a network processor.

The internal transmit state machine will be activated by the rising edge of PA_PE, the falling edge will deactivate it. The PA_PE envelops the transmit data.

This signal switches the power amplifier (PA) from TX to RX as follows:

PA_PE = high--> TX mode
PA_PE = low --> RX mode

TXDATA (I) Pin 28

This pin is used to transfer serial data or preamble/header data from a MAC or network processor to the baseband processor. The LSB is received first and the data is clocked in the baseband processor at the falling edge of TXC. A data bit high = “one”.

TXC (O) Pin 33

Output clock signal to the MAC or network processor used to input serial data to the baseband processor. The data is clocked into the baseband processor using the falling edge of TXC.

TX_RDY (O) Pin 67

Output to the MAC or network processor which indicates that the preamble or header has been generated. This signals that the baseband processor is ready to receive serial data for transmitting over the TXDATA serial line from the MAC or network processor.

TX_RDY signal returns to the inactive state when the PA_PE indicating end of transmission.

CCA (O) Pin 62

Clear Channel Assessment signal indicates the availability of the channel for transmission. The CCA algorithm is user programmable. The detailed operation of this pin may be found in the PRISM Baseband Processor data sheet [5]. The active level of this signal is programmable.

RXDATA (O) Pin 63

Output to a MAC or a network processor which transfers demodulated header information and data in serial format. The LSB is sent first and is aligned with the MD_RDY signal (see Figure 7).

RXCIN (O) Pin 36

This clock signal is used to serially transfer the header and data from the RXDATA pin to the MAC or network processor. The signal is held low when not transferring data.

MD_RDY (O) Pin 59

Signal to a MAC or network processor indicating a data packet is ready. The signal envelopes the data transfer over the RXD serial line.

RX_PE_BB (I) Pin 12

When set high the baseband processor is in receive mode.

SD/SYNTH_DATA (I/O) Pin 30

There are two purposes for this pin. In regards to the baseband processor, this serial line is used to transfer address and data to and from the baseband processor. The MSB is always transferred first. In regards to the synthesizer, the address and data are programmed through this line. The MSB is always first (see Figures 3 and 4).

CLK/SYNTH_CLK (I) Pin 20

This signal is used for serial bus transfers to program the baseband processor and the synthesizer. The data is clocked on the rising edge of the signal at a maximum rate of 10MHz. Even though, CLK/SYNTH_CLK are low frequency, rise and fall times of less than 10ns should be observed.

BB_AS (I) Pin 13

Address strobe is used to envelope the address or the data on SD/SYNTH_DATA while programming the baseband processor. When high, it envelops the address bits. When low, it envelops the data bits (see Figures 2 and 3).

BB_RD/WR (I) Pin 19

Used to change the direction of the SD/SYNTH_DATA line while programming the baseband processor. This signal must be set up prior to the rising edge of CLK/SYNTH_CLK.

BB_CS (I) Pin 14

Active low signal. Baseband processor Chip select signal. When inactive, the signals BB_AS and BB_RD/WR become don’t cares.

RESET_BB (I) Pin 26

Active low signal. Baseband processor reset. Must be inactive during programming. When active RX and TX functions are disabled (see Figure 5).

RADIO_PE (I) Pin 24

This signal, when asserted high, enables the radio card. Power is applied to all chips.

This signal should be kept high during operation of this card.

SEL0 (I) and SEL1 (I) Pins 22, 23

Select the cutoff frequency for the low pass filters in HFA3724 used before going into the Modulator/Demodulator circuit.

SEL1	SEL0	Cutoff Frequency
LO	LO	2.2MHz
LO	HI	4.4MHz
HI	LO	8.8MHz <-- used for 2 Mbps DQPSK, 11 chips
HI	HI	17.6MHz

TX_PE (I) Pin 29

This signal, when asserted high, enables the transmit section of the Modulator/Demodulator and RF/IF Up/Down converter circuits.

RX_PE (I) Pin 27

This signal, when asserted high, enables the receiver section of the Modulator/Demodulator and RF/IF Up/Down converter circuits.

SYNTH_LE (I) Pin 21

SYNTH_LE, CLK/SYNTH_CLK and SD/SYNTH_DATA signals are used to program the synthesizer. SYNTH_LE latches a frame of 22 bits after it has been shifted by the CLK/SYNTH_CLK into the synthesizer registers. Please note that the clock and data lines are shared also by the baseband processor.

OSC_START (I) Pin 11

This signal is an active low pulse which starts the VCO (see Figure 5).

SYNTH_LD (O) (Future Use) Pin 43

Lock detect signal coming back from synthesizer or network processor can contain logic where it will not transmit without a valid lock detect.

RADCLK (I) (Future Use) Pin 41

This signal can provide separate clock to synthesizer, if needed.

TX_PE3 (I) (Future Use) Pin 42 and SPCSPWR (I) (Future Use) Pin 40

These signals are provided for future advanced power management and/or transmit control schemes.

Radio Card Programming

Programming Sequence

1. At power up, set all input signals to default values, see Table 1.
2. Set signal values to baseband processor programming mode (see Figures 2, 3).
3. Program baseband processor as specified in technical data sheet. Example is provided below.
4. Set signal values to synthesizer programming mode (see Figure 4).
5. Program synthesizer as specified in technical data sheet. Example is provided below.
6. Start TX or RX sequence.

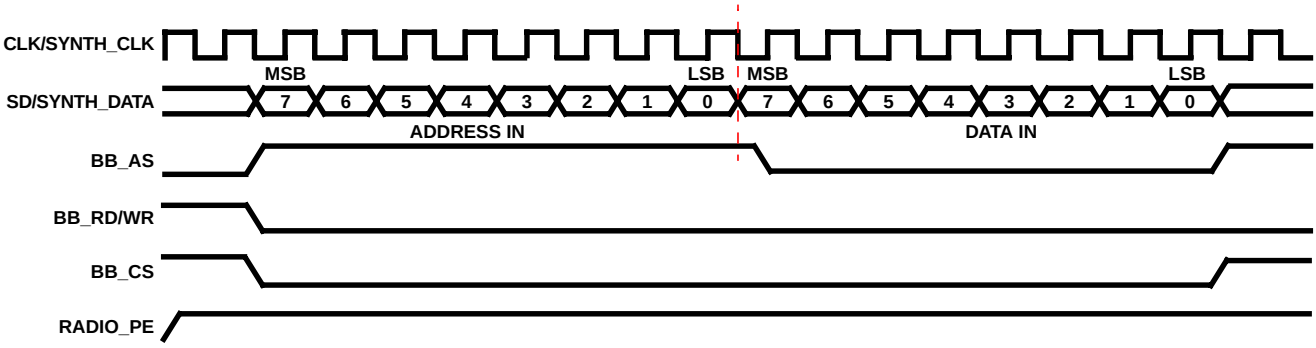
Important - If power is removed from the card, all set ups will be lost.

All (I) signals are input signals into this card. These signals are assumed to be controlled by a MAC (Media Access Controller) and are to be programmed as specified.

Examples are provided as reference only.

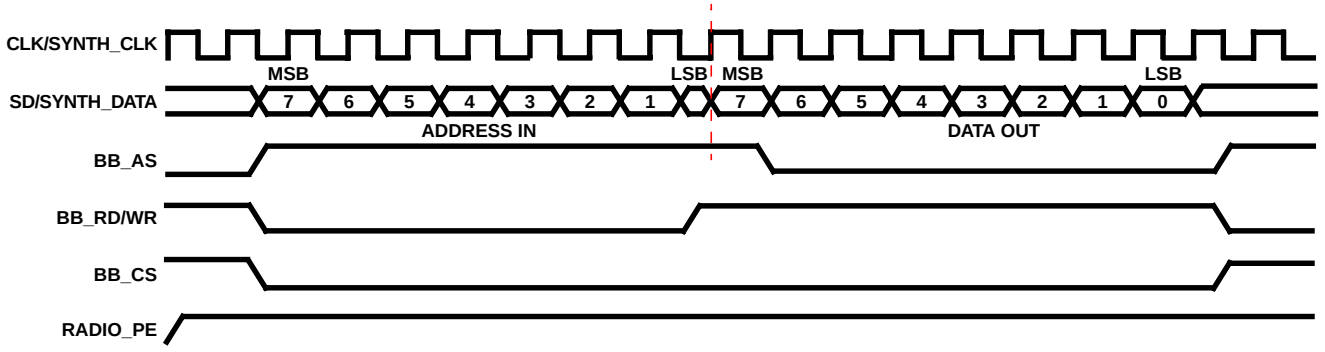
TABLE 1. CONTROL SIGNAL DEFAULT VALUES

CONTROL SIGNAL	VALUE
PA_PE(I)	Low
TXDATA(I)	Do Not Care
RX_PE_BB(I)	Low
SD/SYNTH_DATA(I/O)	Do Not Care
CLK/SYNTH_CLK(I)	Low
BB_AS(I)	Do Not Care
BB_RD/WR(I)	Do Not Care
BB_CS(I)	High
RESET_BB(I)	High
RADIO_PE(I)	High
SEL0(I)	Do Not Care
SEL1(I)	Do Not Care
TX_PE(I)	Low
RX_PE(I)	Low
SYNTH_LE(I)	Low
OSC_START(I)	High



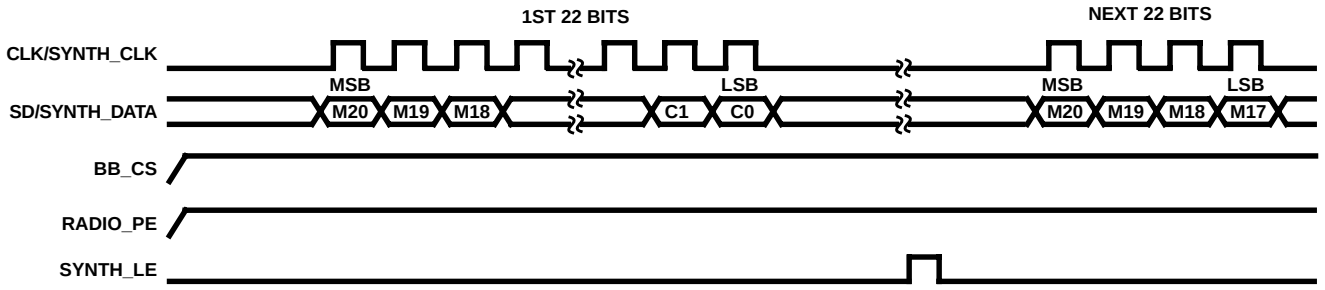
NOTE: Check baseband processor data sheet for timing details.

FIGURE 2. BASEBAND PROCESSOR CONTROL PORT WRITE TIMING



NOTE: Check baseband processor data sheet for timing details.

FIGURE 3. BASEBAND PROCESSOR CONTROL PORT READ TIMING



NOTE: Check synthesizer data sheet for timing details. When the synthesizer is powering up or coming out from Power Down Mode, some registers should be written into it first; refer to the HFA3524, HFA3524A data sheet. After that, the synthesizer is in Power Up mode and it can be programmed according to the data sheet.

FIGURE 4. SYNTHESIZER PROGRAMMING

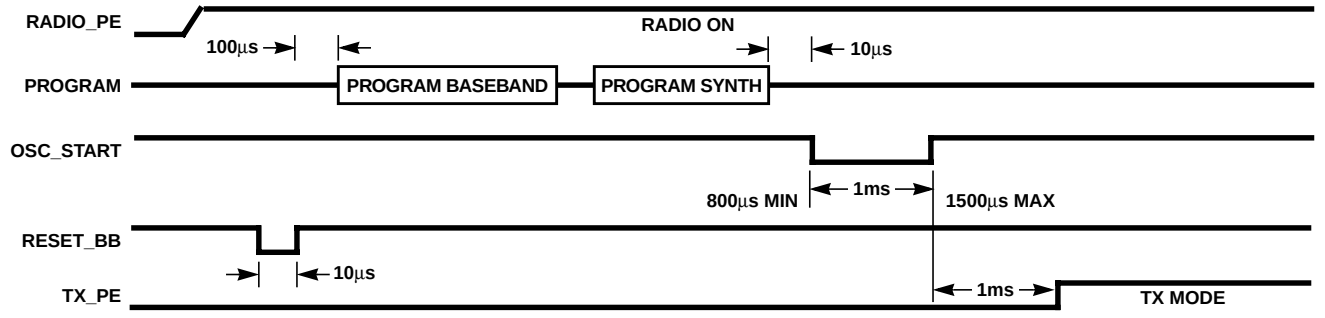


FIGURE 5. PROGRAM SEQUENCE

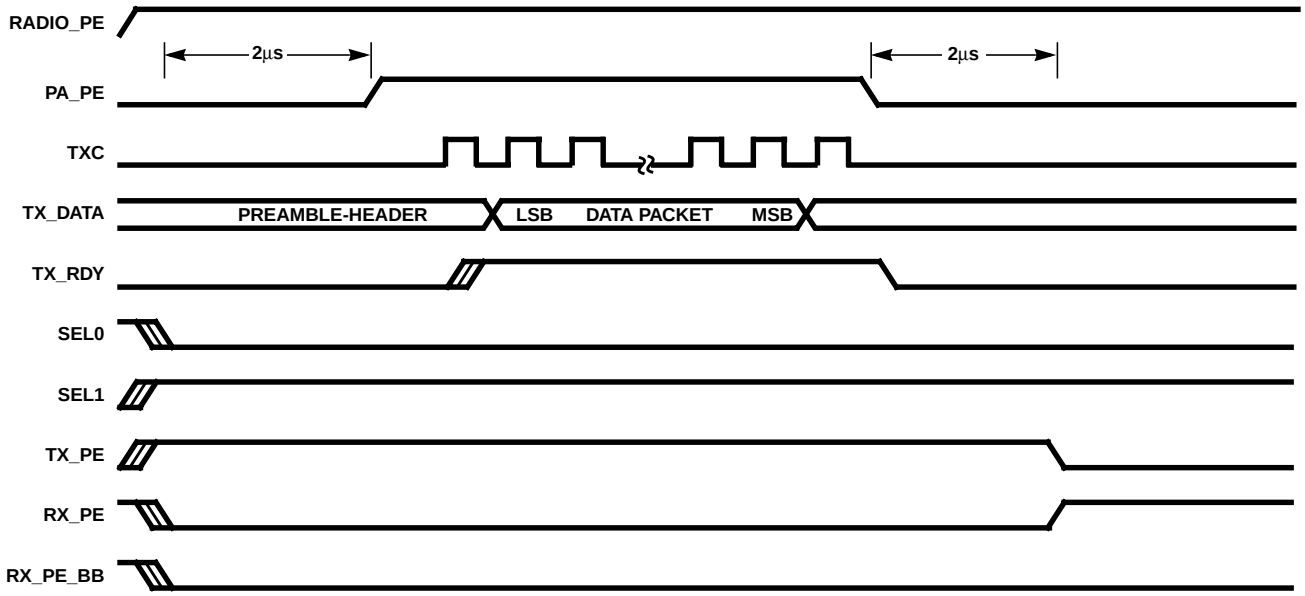


FIGURE 6. TX MODE TIMING

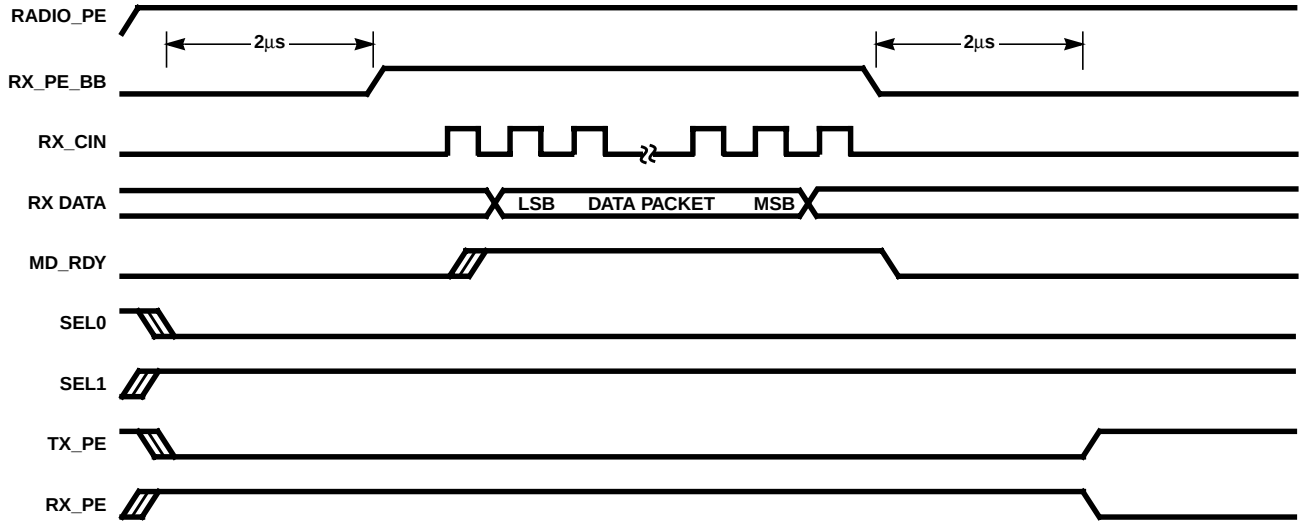


FIGURE 7. RX MODE TIMING

Programming Examples

Example for baseband processor HFA3824A continuous transmit mode programming (Table 2).

TABLE 2.

REGISTER NAME	HEX VALUE	COMMENT
CR0	00	Preamble + SFD Field
CR1	00	
CR2	04	11 Chips/Symbol for RX
CR3	04	11 Chips/Symbol for TX, DQPSK
CR4	00	
CR5	00	
CR9	00	I/O Definition
CR11	01	A/D Cal. Positive
CR12	FD	A/D Cal. Negative
CR13	05	TX Spread Sequence
CR14	B8	
CR15	7F	TX Scrambler Seed
CR16	48	TX Scrambler Tap
CR19	1E	RSSI Threshold
CR20	05	RX Spread Sequence
CR21	B8	
CR22	01	Rx Quality 1 Acq. Threshold
CR23	E8	
CR26	0F	Rx Quality 1 Data Threshold
CR27	FF	
CR30	00	Rx Quality 2 Acq. Threshold
CR31	CA	
CR34	09	Rx Quality 2 Data Threshold
CR35	80	
CR39	5C	
CR41	90	SDF Search Time
CR42	0A	DBPSK Signal
CR43	14	
CR49	F3	SDF Data
CR50	A0	
CR51	00	Tx Service Field
CR56	80	TX Preamble Length

Example for synthesizer (HFA3524A or HFA3524) programming CH1 (RF and IF)

IF R Counter (Read in MSB First)

LSB MSB

0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

C1C2	R	16 17 18 19 20

R16 = 1 --> IF positive
R17 = 0 --> Low current
R18 = 0 --> D_{OUT} IF normal operation
R19 = 0, R20 = 0 --> F_O/LD disable

IF N Counter

LSB MSB

1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	0

C1C2	A	B	P, 20

F_{VCO} = [(P x B) + A] x 22MHz/R <-- see IF R counter set up for “R” value.
IF_{VCO} = [(16 x 023H) + 0] x 22MHz/(16H) = 560MHz
N19 = P = 1 --> /16
N20 = 0 = IF powered

RF R Counter

LSB MSB

0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

C1C2	R	16 17 18 19 20

R16 = 1 --> RF positive
R17 = 1 --> High current
R18 = 0 --> D_{OUT} RF normal operation
R19 = 0, R20 = 0 --> F_O/LD disable

RF N Counter

LSB MSB

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0

C1C2	A	B	P, 20

F_{VCO} = [(P x B) + A] x 22MHz/R
RF_{VCO} = [(32 x 42H) + 14H] x 22MHz/(16H) = 2.132GHz
N19 = P = 0 = /32
N20 = 0 = RF powered

Please check synthesizer technical data sheet (HFA3524A or HFA3524) [7] for more information.

See Table 3 for channel frequencies.

TABLE 3. OPERATING CHANNELS FREQUENCY

CHANNEL ID	FCC CHANNEL FREQUENCIES	JAPAN FREQUENCY	ETSI CHANNEL FREQUENCIES (EUROPE)
1	2412MHz	N/A	N/A
2	2417MHz	N/A	N/A
3	2422MHz	N/A	2422MHz
4	2427MHz	N/A	2427MHz
5	2432MHz	N/A	2432MHz
6	2437MHz	N/A	2437MHz
7	2442MHz	N/A	2442MHz
8	2447MHz	N/A	2447MHz
9	2452MHz	N/A	2452MHz
10	2457MHz	N/A	2457MHz
11	2462MHz	N/A	2462MHz
12	N/A	2484MHz	N/A

Antenna

The antenna connectors are the Huber Suhner 82MMCX - S50 - 2/111KE. The adapter recommended for SMA connector is the Huber Suhner 33MMCX - SMA - 50 -1.

Antenna select should be programmed by programming HFA3824A (bits 6 and 7 in the Configuration Register 0).

See the Radio Card Outline for antenna location.

General Notes

1. This card has been tested and adjusted for operation in Direct Sequence Spread Spectrum. Operation frequency is in the 2.4GHz band.
2. Power spectrum output was checked for CH1 and CH12.
3. The power output was calibrated to +15dBm and link test was conducted with Microsoft Windows™ for Workgroups. The operation range is estimated up to 300 ft. for indoor use.
4. ***Always have a 50Ω load installed in the antenna connectors. If the connector is left open it could cause permanent damage to the power amplifier.***

5. The baseband processor MCLK and the synthesizer are driven by two 22MHz oscillators. Please use this frequencies when programming either device.
6. If this card is inserted in a PCMCIA slot by accident it will not enable card detect, therefore no damage to card will occur.

Abbreviations

(I) = Input to the Radio Card

(O) = Output from the Radio Card

MAC = Media Access Controller

TX = Transmit

RX = Receive

High = 5V

Low = 0V

MSB = Most Significant Bit

References

For Intersil documents available on the internet, see web site http://www.intersil.com/
Intersil AnswerFAX (407) 724-7800.

[1] *AN9624 Application Note*, Intersil Corporation, "PRISM™ DSSS PC Card Wireless LAN Description", Carl Andren, Mike Paljug, and Doug Schultz (Integrated RF Solutions, Inc.), AnswerFAX Doc. No. 99624.

[2] "2.4GHz Direct Sequence Wireless LAN Cascade Analysis", Robert Rood, Doug Schultz, Proc. of the Sixth Annual Wireless Symposium, pp. 532-540.

[3] *AN9665 Application Note*, Intersil Corporation, "PRISM™ Power Management Modes" Carl Andren, Tim Bozych, Bob Rood and Doug Schultz (Integrated RF Solutions, Inc.), AnswerFAX Doc. No. 99665.

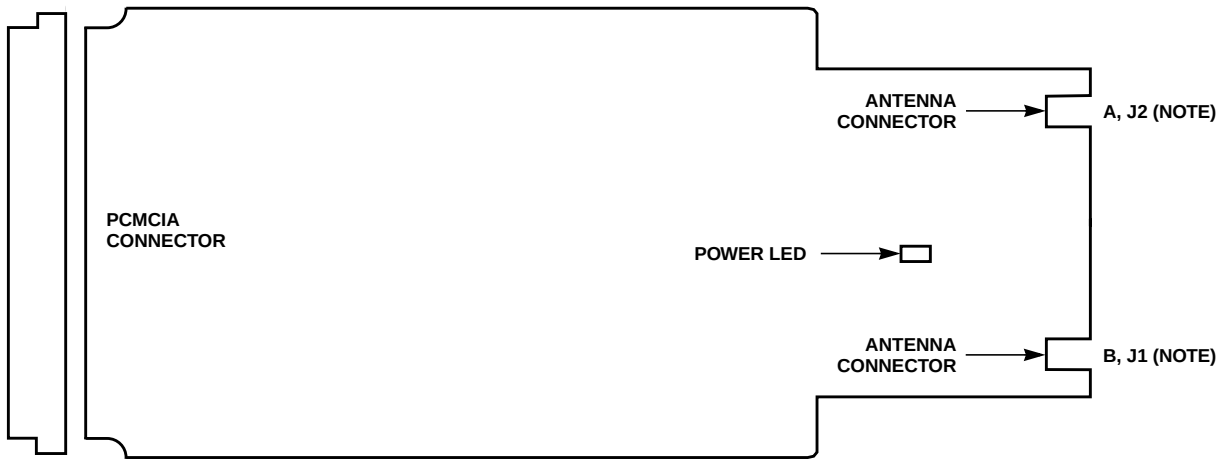
[4] *AN9790 Application Note*, Intersil Corporation, "PRISM™ PC Card Wireless LAN Evaluation Kit User's Guide" Bill Garon, AnswerFAX Doc. No. 99790.

[5] *HFA3824A Data Sheet*, Intersil Corporation, "Direct Sequence Spread Spectrum Baseband Processor", AnswerFAX Doc. No. 4459.

[6] *AN9617 Application Note*, Intersil Corporation, "Hardware/Software Interface Description for PRISM™ Radio Design with an Example Using the AM79C930 Media Access Controller", John Fakatselis and Mike Paljug, AnswerFAX Doc. No. 99617.

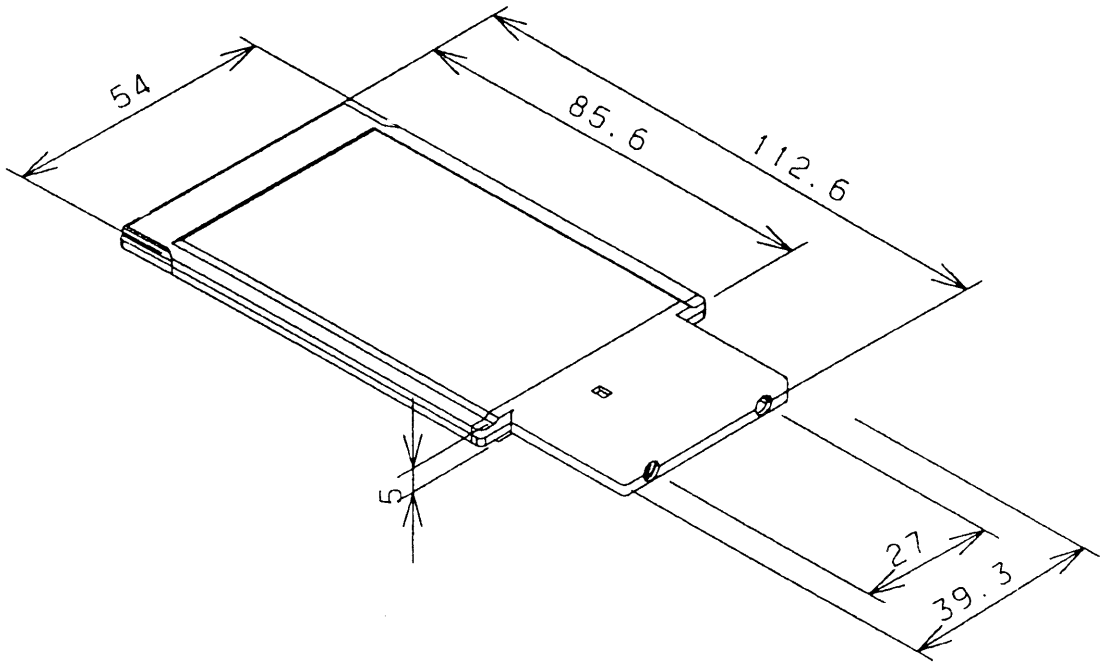
[7] HFA3524, HFA3524A Data Sheet, Intersil Corporation, "2.5GHz/600MHz Dual Frequency Synthesizer", AnswerFAX Doc. No. 4062.

Radio Card Outline - Top View



NOTE: A and B refer to Baseband Processor HFA3824A data sheet [5], J1 and J2 (refer to PRISM1RC schematic).

Radio Card Dimensional Outline



NOTE: Units are in millimeters.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029